High Power Force Oscillator and Drive Electronics

O. Sosnicki; A. Pagès; M. Hihoud; F. Claeyssen.
Cedrat Technologies S.A. 15 chemin de Malacher, Inovallée, 38246 Meylan Cedex, France
Phone: +33 (0)4 76 90 50 45 ; Fax: +33 (0)4 56 38 08 30

Abstract:
This paper presents the development of one amount the largest piezo actuator ever designed based on low voltage PZT. This actuator is able to provide more than 20kN of force in dynamic operation (60kN in static operation). The purpose of low frequency vibration generation is to improve the quality of parts production in the field of manufacturing and machining process.
Such an actuator requires high power electronics to drive it to its maximum performances. In that regard high switching power amplifier, namely the SA75D, has been developed. The SA75D is a new high power amplifier dedicated to supply piezo-electric actuators. Using high frequency PWM techniques with a specific topology for piezo-electric loads, the SA75D offers large power, very low ripple, and allows energy harvesting in a small volume. These special features make the SA75D perfect for dynamic and precise motion applications
The paper presents the development of both actuator and electronics, including simulation, design and tests results.

Keywords: Large piezo actuator, force oscillator, stick-slip reduction, high power piezo driver, FP7 Learnform.

Introduction
The use of additional vibrations in manufacturing processes aims at improving the quality of the parts in certain conditions. In sheet metal forming for instance, it has been shown that the use of additional dynamic forces reduced the stick-slip effect leading to crack avoidance during the process. Such experiments were realised using hydraulic cylinders at low frequencies (10Hz). This benefit has never been studied at higher frequency since the ability to produce large force at higher frequency cannot be addressed by hydraulic jacks.
The purpose of this paper is to present the design of a large piezo actuator. This force oscillator (FO) shall be able to withstand large external loads, according to the process, and shall provide significant forces at relatively high frequency (200Hz). Since the dynamic performances of the actuator are strongly coupled with the electrical power supplied to the piezo components, this study fully describes the development of a high power amplifier called SA75D.

Principle
Force oscillator shall provide additional dynamic forces during a process. Two possible configurations are proposed at this stage: Inline actuator configuration is the simplest way to integrate a FO in between a mechanical clamp. The force generated by the actuator is then directly transmitted to the clamp as long as the overall system is rigid enough with respect to the FO. In this configuration, both static and dynamic forces can be transmitted toward the targeted part.
However, the FO is submitted to large external forces provided by the process.
Proof mass actuator configuration, is less compact than the inline one. In this case the FO is not submitted to large external forces provided by the process. Although this configuration only allows dynamic forces generation, the mechanical transmission does not required rigid clamping of both side of the FO. These two configurations are then considered in the study. The FO should be compatible with both configurations.
The use of low voltage piezo actuator is preferred in this study. Two possible designs are proposed to get large force generation: The first one uses one single large multilayer actuator. The maximum possible size of such a component is strongly dependant to fabrication process. The state of the art ever built and integrated in this study has the following dimensions: Inner diameter 10.5mm; outer diameter 45mm. The second uses a combination of several stacks of piezo components equi-spaced in a parallel mounting. Both components are shown Fig. 1:

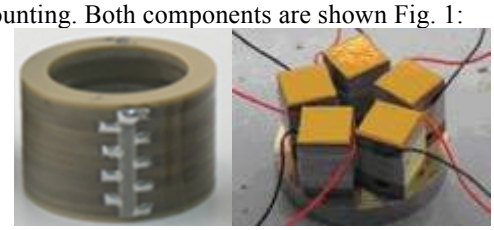

Fig. 1 *Low voltage piezo components; Large MLA (left) Standard piezo stacks (right)*

Force oscillator description
The concept of force oscillator comprises an active material, a preloading element, a flexural hinge, two deformable membranes and a mechanical housing.
The active material is mounted in suspension thanks to the use of membranes inside the housing. This

integration allows backlash free when the actuator is mounted and clamped in functional operation. The flexural hinge is necessary to prevent any angular misalignment from bending the piezo active element. The mechanical interfaces are then defined (Fig. 2)

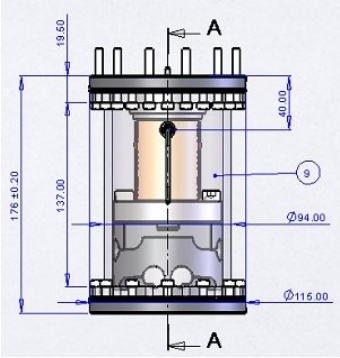

Fig. 2 *Force oscillator design*

Mechanical analysis

A mechanical analysis is performed to ensure the mechanical frame allows to withstand external loads . Meanwhile, the stiffness matrix of the force oscillator is computed by Finite Element Method .Predicted performances are 60µm stroke and a 26.6kN blocked force. The FO withstands 0.1 degree angle and 1mm backlash free. Only 70% of the piezo element blocked force is produced by the FO in order to withstand angular misalignment of (+/- 0.1) degree.

Prototyping & characterisation

The prototype of FO is integrated and tested at sub system level. The admittance test is useful to extract eletromechanical parameters. The resonance frequency is measured at 4300Hz. The model can then be raised (Fig. 3).

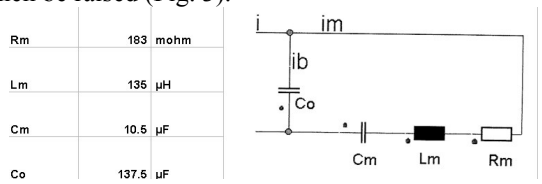

Fig. 3 *FO electromechanical model*

A dummy FO equipped with strain gauges is prototyped in order to evaluate the tensile stress that occurs within the piezo element when the system is loaded with a 0.1 degree misalignment. A dedicated bench that provides 60kN of force is built to perform this stresses evaluation. The results are promising since the maximum tensile stress measured within the piezo stack is withstood by the preload element. Indeed, the 15MPa of preload realised by the tensile stud overcome the tensile force produced by both loading and angular misalignment. At this stage of the characterisation the FO displays a perfect protection for piezo stack to external efforts and produces 28kN of blocked force.

Drive Electronics impact and requirements

This new force oscillator is defined by a large electrical capacitance. By adding high force requirement corresponding to large bandwidth, the drive electronics is a challenge: Full mechanical actuation at a minimum of 200Hz. Basically, a piezoelectric mechanism could be represented by the well established electromechanical model (Fig. 3).

This model is characterised by the motional branch and the electrical branch. The first one was studied in the previous paragraphs. From the electronics point of view, the large capacitance coupled with the required bandwidth is THE difficulty. To use the inherent advantages of the piezo actuator to move very fast and to provide high force, the required movement shall be characterised by short settling time like square pulse or high frequency sine signals. In this case and if the actuator is able to provide the needed force, the acceleration will be very high (i.e the associated generated force) only if the ratio stroke amplitude - rise/fall time is very high. This last property is very important and depends on two factors: The first one is the mechanical design of the mechanism and the second one the electronics capability to provide enough power to the piezoelectric load. As this load is similar at the first order to large capacitances, a short settling time is characterised by a high current flow [Equ 1]

$$i_{load}(t) = C\frac{\partial v_{load}(t)}{\partial t} \qquad \text{Equ 1}$$

In the case where a square pulse signal is chosen the required force given is 23kN, the computed acceleration is 167G (assuming an embedded mass of 7 kGrams). The corresponding rise/fall time needed is 600µs (if full stroke is reached).

When considering to the equivalent capacitance of the piezo mechanism, the specification is to provide more than 30Amp peak current to the load during the settling time. For the rest of the study, with a applied voltage of 170Vpeak to peak (centred on an offset 65V), we will assume that the delivered reactive power will be up to 1.9kVA.

Proposed topology for the electronics driver

Based on these first considerations, the choice of the topology for the driver is done by taken into account that the large current flow necessitates switching amplifier. The other category of amplifiers (the linear amplifiers) implies large losses during the operating that are not manageable with the transistors, which work like resistors. On the contrary, in the switching amplifier, the transistors work like interrupts with only two states ON and OFF characterised by 2 resistances values: Null and infinity. The improvements in this domain allow reduction of losses. Another aspect is the energy harvesting possibility in a properly configured switching amplifier: As the load is characterised by

a large reactive behaviour, the active power is very light and only due to the capacitance and mechanical losses. With the 1.9kVA, only 5-10% is powered from the AC bus corresponding of 190W on the primary side. A large capacitive buffer is added on the AC-DC converter to take advantage of this harvesting technique [1]. The mechanical power required is 1.9kWatt. Several topologies exist to design these kinds of switching amplifiers like resonant or Pulse Width Modulation converter. The overall bandwidth is quite large (and the repeating frequency is not well known), a configuration working with small bandwidth around a specified frequency is not sufficient to address different frequencies/settling times and the resonant configuration is not chosen [1]. The PWM converter is well adapted to answer to a broad bandwidth. The PWM converter is defined by a PWM generation, a power output stage, an output filter and a feedback network (***Fig. 4***). It includes an AC-DC converter to provide the BUS voltage.

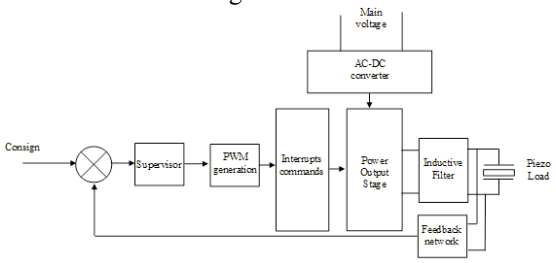

Fig. 4 *Synoptic of PWM converter*

The AC/DC converter is not the principal function of this study. The chosen topology is based on a Flyback converter. Thanks to the reactive behaviour of the piezo load, in counterpart, the active power is very small and the Flyback converter is well adapted to convert the AC main to a DC high voltage.

The chosen PWM inverter topology shall present low loss and additionally, to improve the total harmonic distortion (i.e., to limit the stress into the multilayer ceramic). A study has been performed to analyse the impact of the cut-off frequency of the output filter, the stability of the driver with its voltage feedback and the attenuation at the switching frequency. As the piezo actuator is characterised by a small mechanical Q-factor, the design of the output filter (frequency and attenuation) is managed by a reduction of stress due to the magnification of the residual spikes. This could excite the piezo resonances. Three topologies have been analysed in regards of these parameters: Half bridge, Full bridge and Neutral Point Control with 3 levels

Preliminary Design

Analytic models were used to compare the losses and the open loop Total Harmonic Distortion of these converter topologies. The open loop THD is defined as the THD without any control of the output voltage and is computed. The choice of the reference frequency is restricted both in the upper and the lower end. From the sampling accuracy and the following reconstruction of the analogue signal point of view it is desired to have the highest possible reference frequency. On the other hand, power amplifiers have limited frequency range and they possibly need low pulse rate to amplify without significant shape distortion and power losses in transistors.

As high switching frequency with a high attenuation output filter improves the THD, the design had to use the highest possible switching frequency. 100 kHz (which limits the losses in the interrupts) and a 2nd filter with a cut-off frequency around 2 kHz (directly linked to the settling time of the full stroke) are used for the comparison. Notice that a full bridge converter with a full wave control switches at 200 kHz (for better THD) (See ***Fig. 5***)

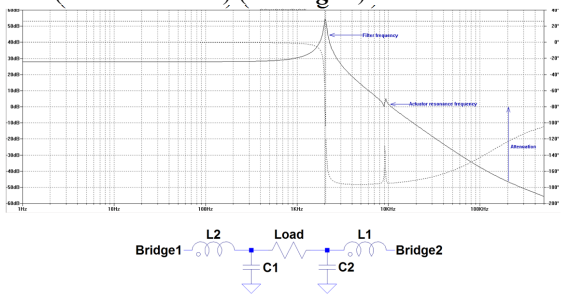

Fig. 5 *Filter frequency position versus the switching frequency and mechanical resonance.*

From these curves, it is clear that the characteristics of the filter are provided by the capacitance value of the piezo actuator: the larger the capacitance, the smaller the bandwidth and the THD.

The losses inside the output stage take into account the interrupts losses, conduction losses, switching losses, the parasite capacitance charge losses, the command losses and, if any, the diodes losses [3]. As the switching frequency is higher than 50 kHz (to improve the attenuation of the switching frequency), MOSFETs with voltage range under 250V are used instead ok IGBTs. A numerical analysis is elaborated taken into account theses remarks (***Fig. 6***).

	Full Bridge	NPC – 3Levels	Half Bridge
	Losses (W)	Losses (W)	Losses (W)
T1	32,4	24,6	42,7
T2	29,1	22,4	38,4
T1'	29,5	10,6	
T2'	32,1	4,81	
D1 Diode		23,2	
D2 Diode		23,6	
Total losses	**123**	**109**	**81,1**

a- Full bridge: 0.89% b- NPC-3levels: 2.98% c- Half bridge: 1.45%

Fig. 6 *Results for the 3 PWM topologies: Total losses and THD behaviors*

Additionally to these technical issues, complexity and volume were studied and a trade off has beendone. Finally the Full bridge configuration was chosen particularity for its good performances in terms of THD and its capabilities to output large

power even if the total losses are quite poor but manageable regarding heat.

Models validation

A SPICE model was built including the different electrical functions. The PWM output is fully floating (coupled with a floating DC voltage Bus from the Flyback converter) and the output filter is defined as a differential filter to reduce EMI problem.

Particular attention is given to the definition of the dead time between the commutations with each interrupt to limit the risk of cross-conduction while this value is reduced at the minimum to improve the distortion. Dead time around 100ns is chosen as first value. The rules definition of the output filter is based in the previous study and is recalled in [1]. To analyse the behaviour of the full bridge PWM converter, two analyses have been carried out: the open loop analysis and the impact of the feedback network with the supervisor in closed loop (Fig. 7).

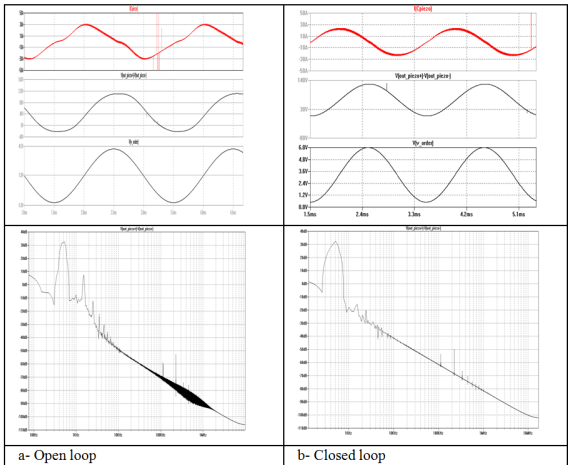

Fig. 7 *Transient and THD computation results of the Full bridge PWM converter: Open loop and Closed behaviours with sine signal excitation*

As pulsed square signal is able to excite the electrical resonance of the output filter in open loop, the rise-fall times are limited to 1ms to limit this phenomenon. Among the results, the simulations showed the capabilities of the output stage to provide large current with large voltage without large distortion as discussed in the previous design paragraphs. The peak current is up to 36Amps during 0.5ms. The closed response allows limiting the overshoot due principally to the feedback network and the supervisor.

From the sine responses, the THD in open and closed are compared. As discussed in the previous paragraph, the THD in open loop is good enough (~ 7.1%). It has to be noted that the residual voltage due to switching frequency is largely attenuated by 10000. When the loop is closed (i.e. the output voltage is compared to the input consign), the THD is improved and reaches 0.5%.

Overall performances

The FO and the drive electronics are integrated into a mechanical press for sheet metal forming (Fig. 8).

To test the Force Oscillator, the overall design includes 2 boards for the AC-DC converter and the full bridge PWM converter with its output filter. All these boards are integrated in a rack named SA75D including the thermal management - Fan & Heat sink.

Care has been taken to limit the parasites components during the routing (large current with small transient could give large EMI radiation/conduction).

Fig. 8 *Picture of the SA75D rack (left), FO integration (middle), FO (Right)*

Conclusions

In proof mass configuration the force oscillator and the SA75D generates 11kN of dynamic force, whereas in inline configuration the FO produces a dynamic sine force of 23kN up to 550Hz. Thanks to the generation of more than 32Amp and 100V, the FO displays high dynamic inertial forces.

Acknowledgment

CEDRAT authors are grateful to Pr Jean-Paul Ferrieux and its team from G2ELab [4] for a significant contribution in SA75D development, and to FP7 LEARNFORM project for funding FO works.

References

[1] C. Kauczor, N. Fröhleke, Inverter topologies for ultrasonic piezoelectric transducers with high mechanical Q-Factor, 2004 35th Annual IEEE Power electronics Specialist conference, Aachen (2004)

[2] D.K Lindner, M. Zhu, Comparison of linear and switching driver amplifier for piezo piezoelectric actuators AAIA (2002)

[3] Jorge Cerezo, International Rectifier, Application Note AN- 1070

[4] Ekaitz Goenaga, Conception et dimensionnement d'un onduleur de puissance à MLI pour les actionneurs piézo-électriques, JCGE2011.